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VG24C04A
2-Wire Serial EEPROM

Data Sheet

Mar. 2025

Trademarks

Description

The VG24C04A provides low operation voltage of 4096 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

Features

- **Low Operation Voltage: V_{CC} = 1.7V to 5.5V**
- **Internally Organized: 256 x 8**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bi-directional Data Transfer Protocol**
- **1MHz (2.5V~5.5V) and 400 kHz (1.7V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **8-byte Page Write Modes**
- **Partial Page Writes are Allowed**
- **Self-timed Write Cycle (5 ms max)**
- **Operating Temperature range: -40° C to +85° C**
- **High-reliability**
  - **Endurance: 1,000,000 Write Cycles**
  - **Data Retention: 100 Years**
- **SOP8 and TSOT23-5L Packages (RoHS Compliant and Halogen-free)**

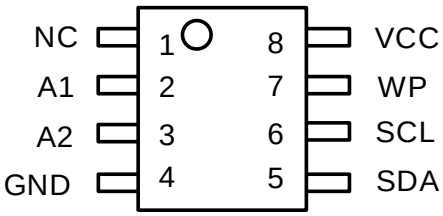
Absolute Maximum Ratings

Ambient Operating Temperature	-55℃ to +125℃
Storage Temperature	-65℃ to +150℃
Voltage on Any Pin with Respect to Ground	-0.5V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

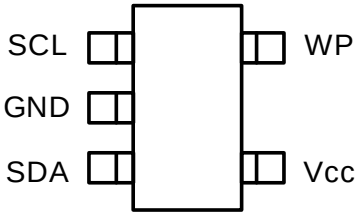
*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Packaging Type

SOP 8



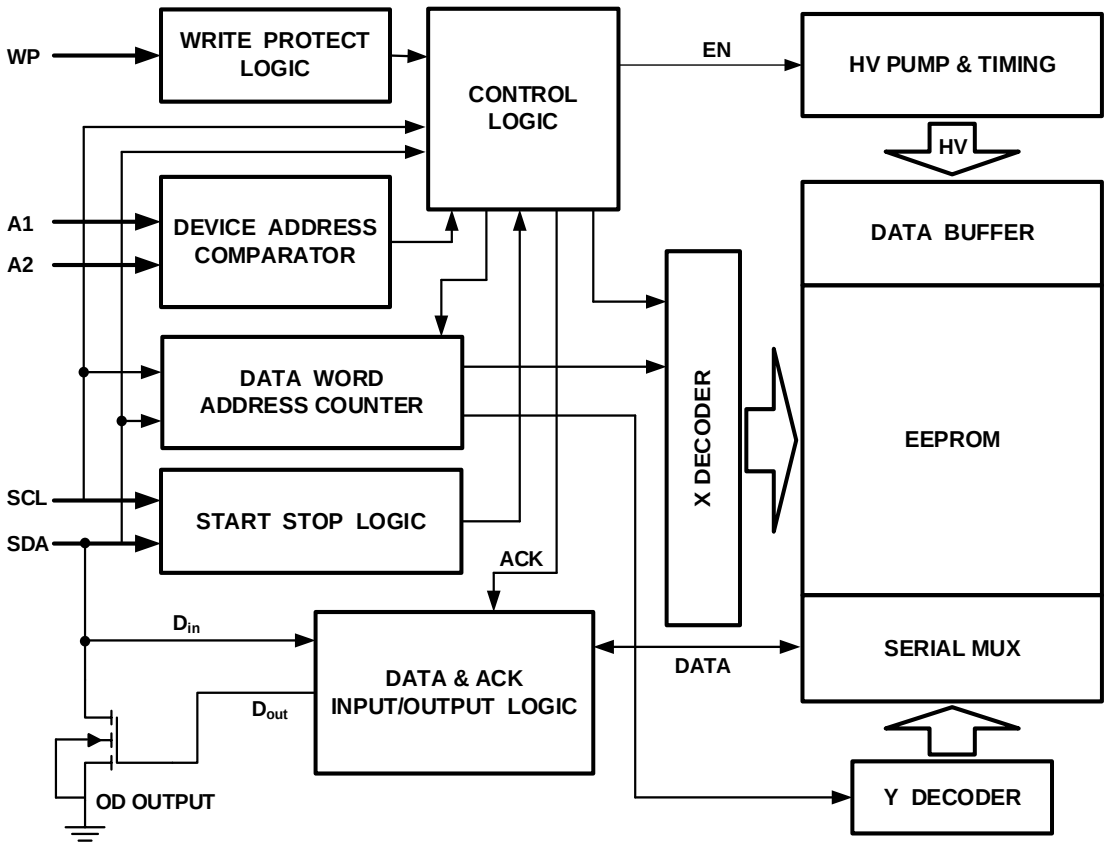
SOT23-5L



Pin Configurations

Pin Name	Function
NC	Not Connect
A1～A2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply
GND	Ground

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1): The VG24C04A uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The NC pin is a no connect and can be connected to ground (device addressing is discussed in detail under the Device Addressing section).

WRITE PROTECT (WP): The VG24C04A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to $V_{CC,}$ the write protection feature is enabled.

Write Protect Description

WP Pin Status	Part of the Array Protected
WP=V_{CC}	Full (4K) Array
WP=GND	Normal Read/Write Operations

Write-protect condition: The WP pin must be connected to V_{CC} from start condition in the write operation (byte write, page write) until stop condition (refer to Figure 11).
Non-write-protect condition: The WP pin must be connected to GND from start condition in the write operation (byte write, page write) until stop condition (refer to Figure 12).

In not using the write protect, connect the WP pin to GND or set it open. The write protect is valid in the range of operation power supply voltage. If the WP pin changes during this time, the address data being written at this time is not guaranteed. Regarding the timing of write protect, refer to Figure 3.

Memory Organization

VG24C04A, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

Pin Capacitance

SYMBOL	PARAMETER	CONDITIONS	Max	Units
C_{IN} (1)	Input Capacitance	V_{IN} = 0V, f = 1MHz	6	pF
C_{OUT} (1)	Output Capacitance	V_{OUT} = 0V, f = 1MHz	8	pF

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V, Read at 400K		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V, Write at 400K		2.0	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V, V_{IN} = V_{CC}/ V_{SS}		3.0	6.0	μA
I_{SB2}	Standby Current	V_{CC} = 5.5V, V_{IN} = V_{CC}/ V_{SS}		8.0	18.0	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}/V_{SS}		0.1	3.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}/ V_{SS}		0.05	3.0	μA
V_{IL} 1	Input Low Level		-0.45		V_{CC} x 0.3	V
V_{IH} 1	Input High Level		V_{CC} x 0.7		5.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.7V, I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from: T_A = -40℃ ~ +85℃, V_{CC} = +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7-volt		2.5-volt		5.5-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.3		1.3		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		0.6		µs
t_{AA}	Clock Low to Data Out Valid	0.2	3.45	0.1	0.9	0.1	0.9	µs
t_{BUF} [1]	Time the bus must be free before a new transmission can Start	4.7		1.3		1.3		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		0.6		µs
$t_{SU.STA}$	Start Setup Time	4.7		0.6		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		0		µs
$t_{SU.DAT}$	Data In Setup Time	250		100		100		ns
t_R [2]	Inputs Rise Time		1.0		0.3		0.3	µs
t_F [2]	Inputs Fall Time		0.3		0.3		0.3	µs
$t_{SU.STO}$	Stop Setup Time	4.0		0.6		0.6		µs
t_{DH}	Data Out Hold Time	200		100		100		ns
t_{WS1}	WP setup time	1		1		1		µs
t_{WH1}	WP hold time	1		1		1		µs
t_{WS2}	WP release setup time	1		1		1		µs
t_{WH2}	WP release hold time	1		1		1		µs
t_{WR}	Write Cycle Time		5.0		5.0		5.0	ms
Endurance [1]	3.3V, 25℃, Page Mode	1,000,000						Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

2. t_R or t_F must rise or fall monotonically without ringback.

3. AC measurement conditions:

RL (connects to V_{CC}): 1.3 kΩ

Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}

Input rise and fall times: ≤ 50 ns

Input and output timing reference voltages: 0.5 V_{CC}

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle. Following receipt each word from the EEPROM, the microcontroller should send a zero to EEPROM and continue to output the next data word or send a stop condition to finish the read cycle.

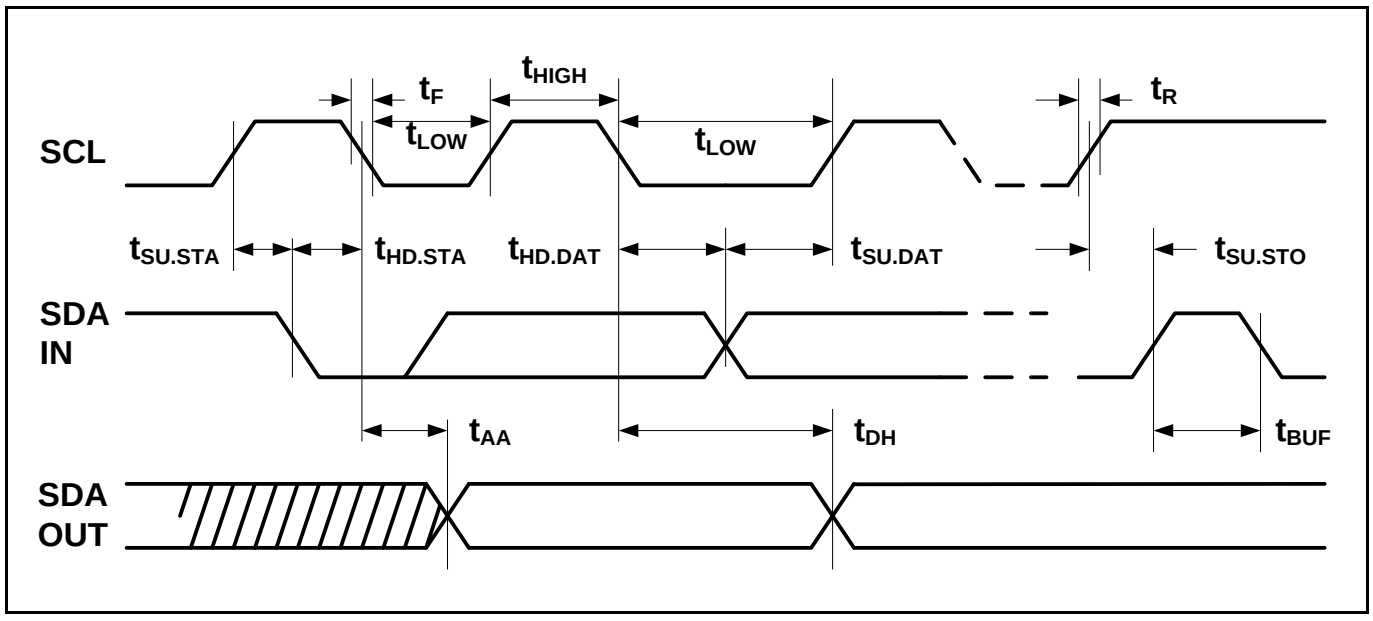
STANDBY MODE: The VG24C04A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

DEVICE RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset in following these steps:

1. Clock up to 9 Cycles,
2. Look for SDA high in each cycle while SCL is high and then,
3. Create a start condition as SDA is high.

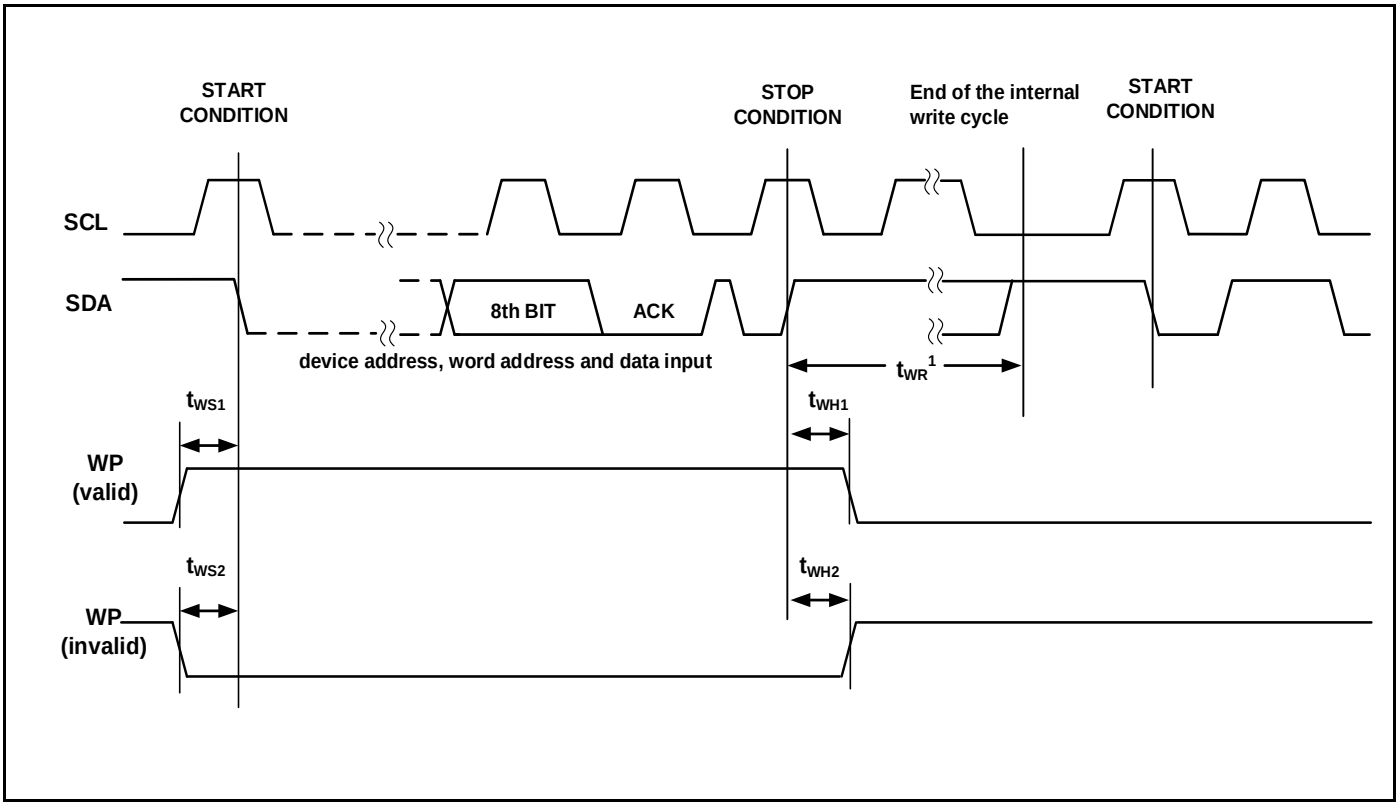
Bus Timing

Figure 2. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 3. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4. Data Validity

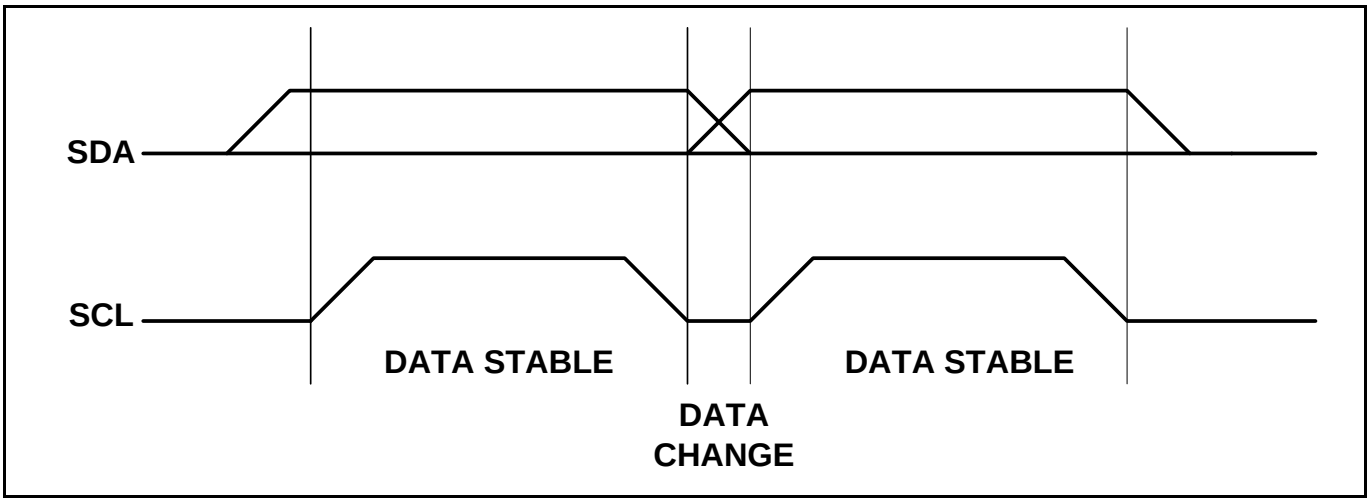


Figure 5. Start and Stop Definition

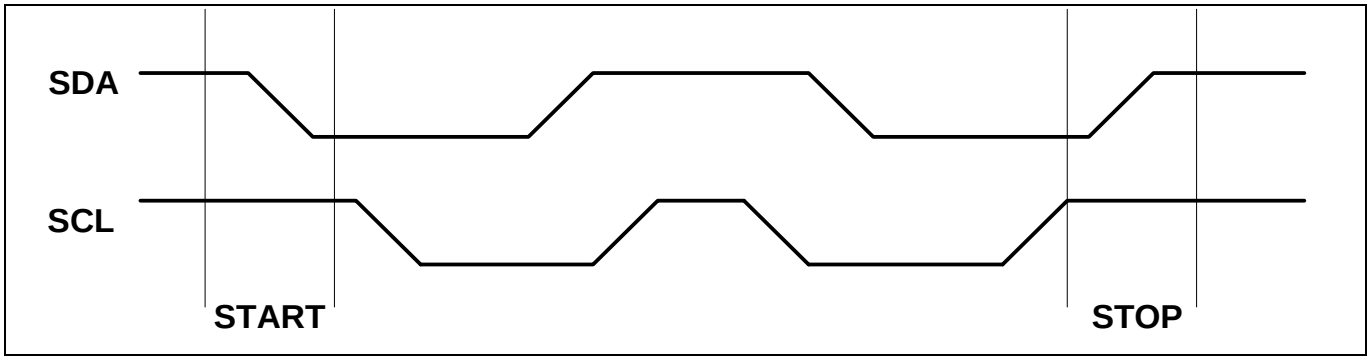
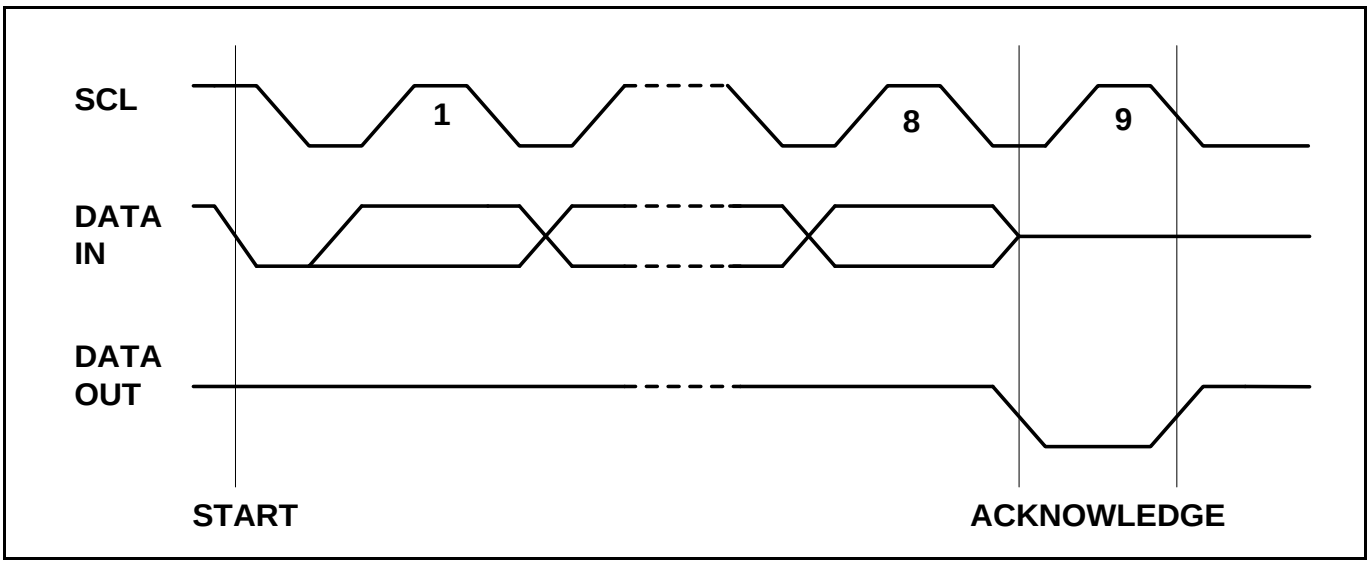
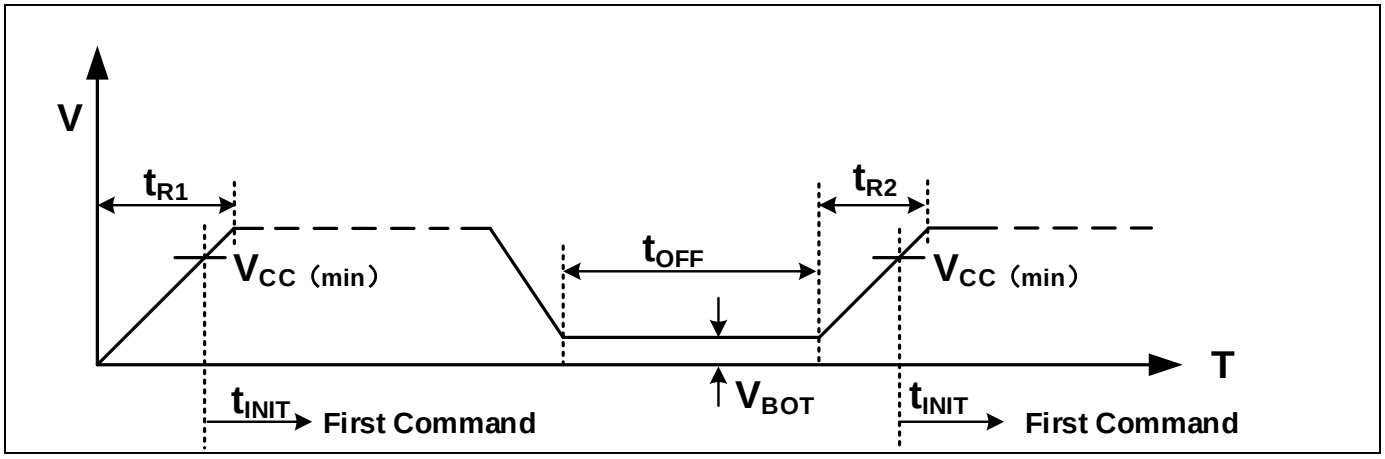


Figure 6. Output Acknowledge



Power-up Timing

Figure 7. V_{CC} Ramp Up and Ramp Down



Symbol	Parameter	Test Condition	Min	Max	Units
t_{R1}	Power on time from 0V			20	ms
t_{R2}	Power on time from V_{BOT}	V_{BOT}≤0.2V		5	ms
t_{OFF}	power cycle off time		50		ms
t_{INIT}	Time from power on to first command		100		us
V_{BOT}	Power Off threshold for the next power on cycle	No ringback above V_{POFF}		0.2	V

Note: VCC must rise monotonically without ringback.

Device Addressing

The 4K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 8).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 pin is no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 9).

PAGE WRITE: The 4K devices are capable of 8-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 10).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 13).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 14).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 15)

Figure 8. Device Address

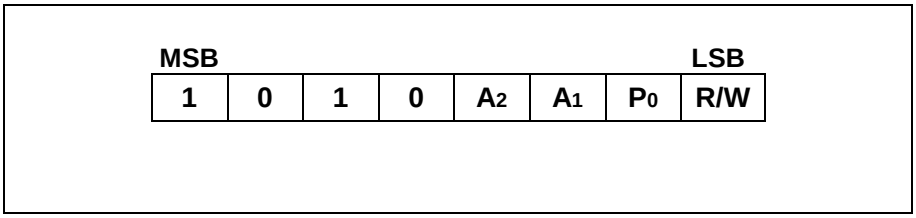


Figure 9. Byte Write

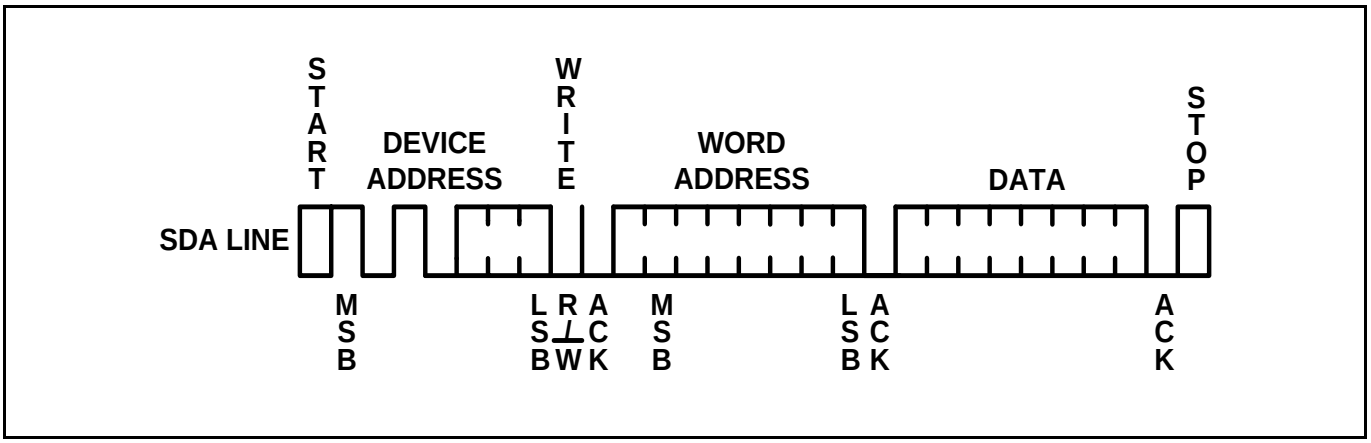


Figure 10. Page Write

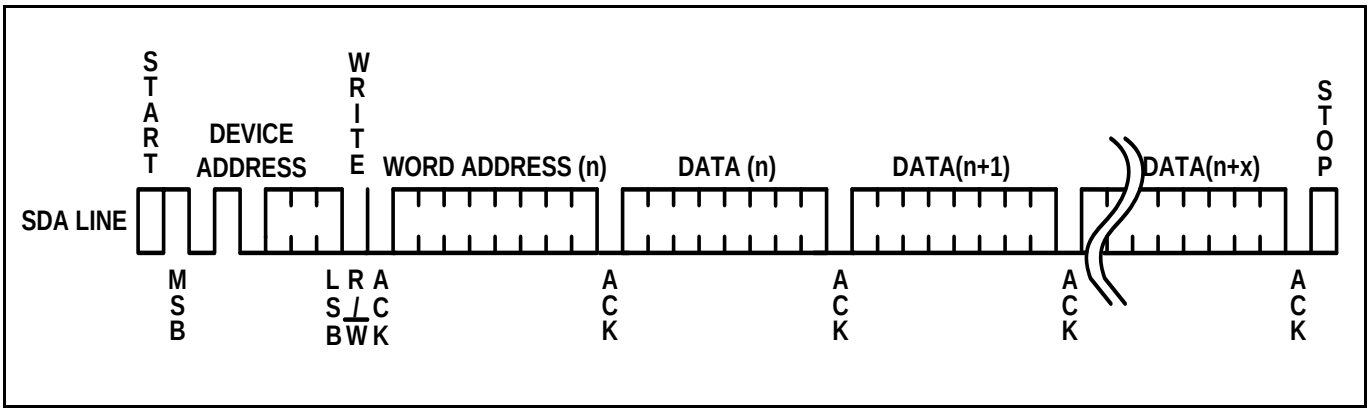


Figure 11. Write-Protect Condition

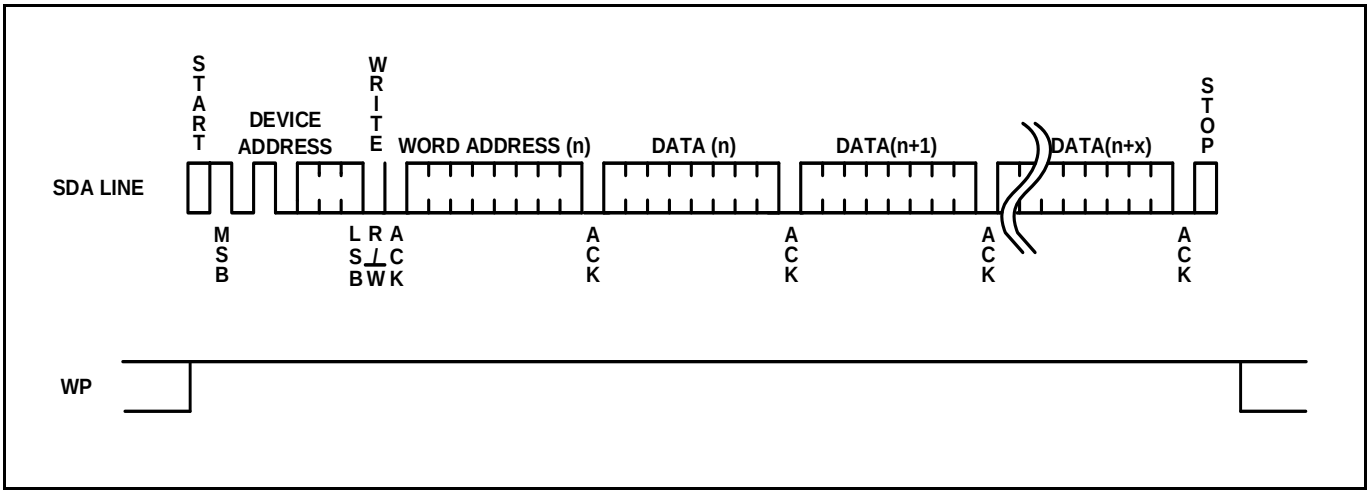


Figure 12. Non-Write-Protect Condition

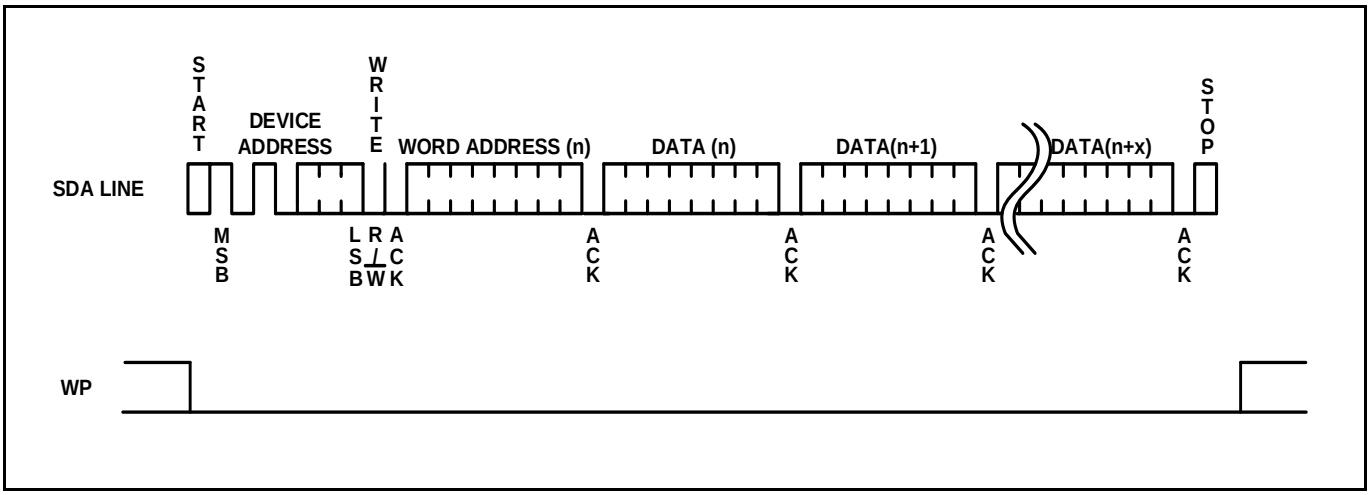


Figure 13. Current Address Read

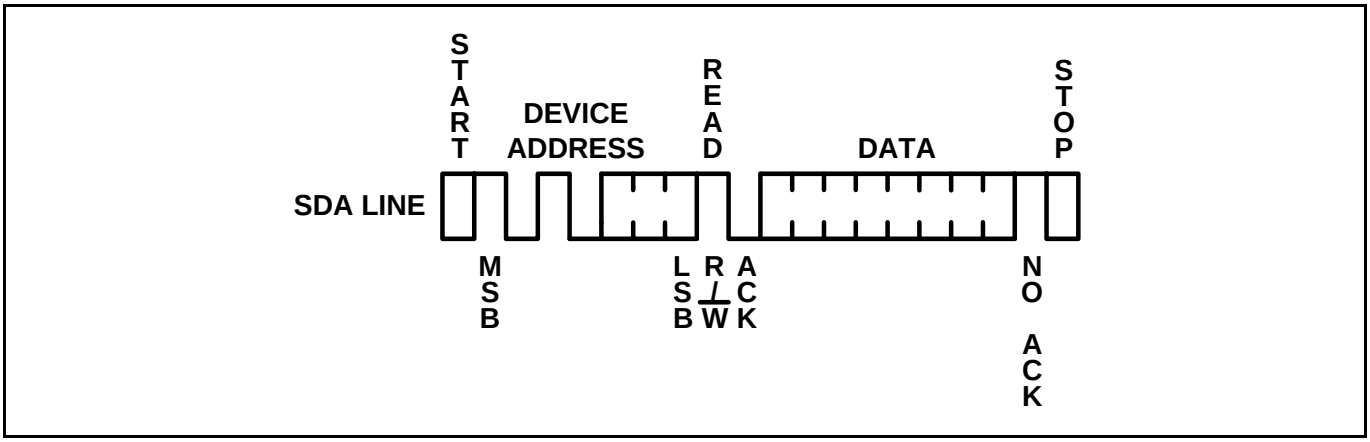


Figure 14. Random Read

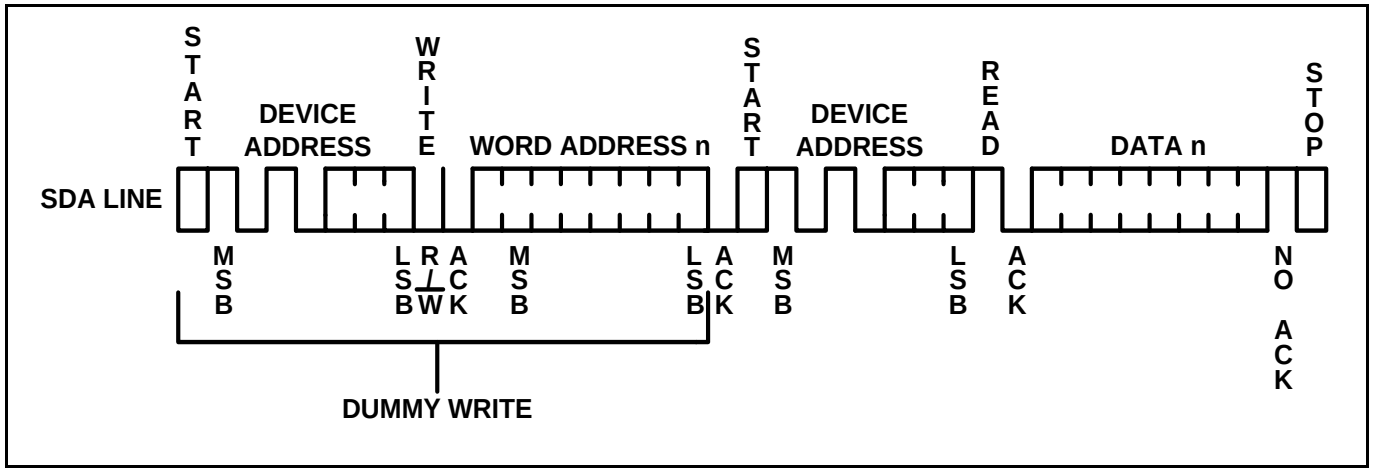
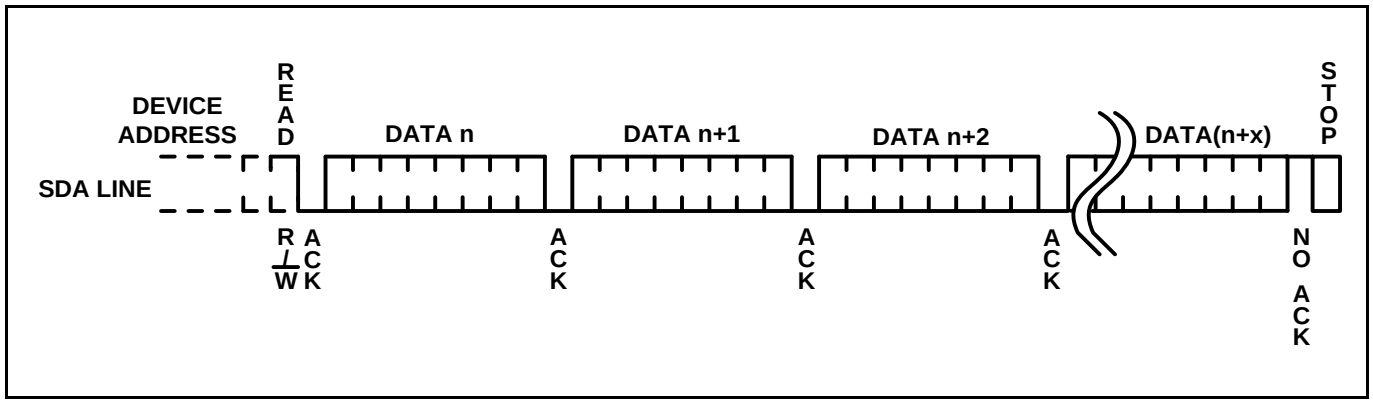


Figure 15. Sequential Read



Ordering Information

VG24C 04 A -PP -C -H

Product Family

VG24C = 2-Wire Serial EEPROM

Product Density

04 = 4K-bit

Supply Voltage

A = Version

Package Type

STA = 5-pin SOT23-5L
SO = 8-pin SOP

Product Carrier

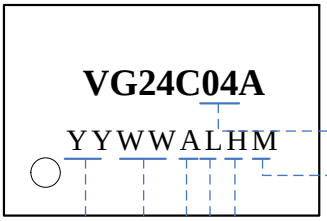
U = Tube
T = Tape and Reel

HSF ID Code (1)

Blank or R = RoHS Compliant
G = RoHS Compliant, Halogen-free, Antimony-free

Part Marking Scheme

SOP8



Product Density

Moisture Sensitivity Level
1 = MSL1
Blank=MSL3

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.

SOT23-5L

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

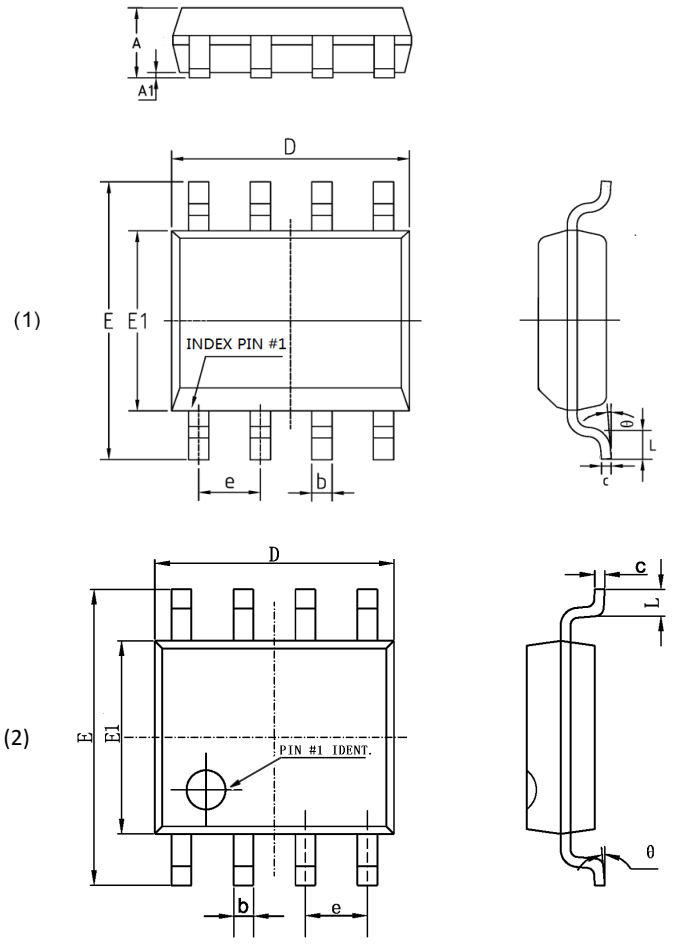
Assembly's Code

The month(hexadecimal digit) in which the product was molded.

The last one digits of the year In which the product was sealed / molded.

Packaging Information

SOP 8

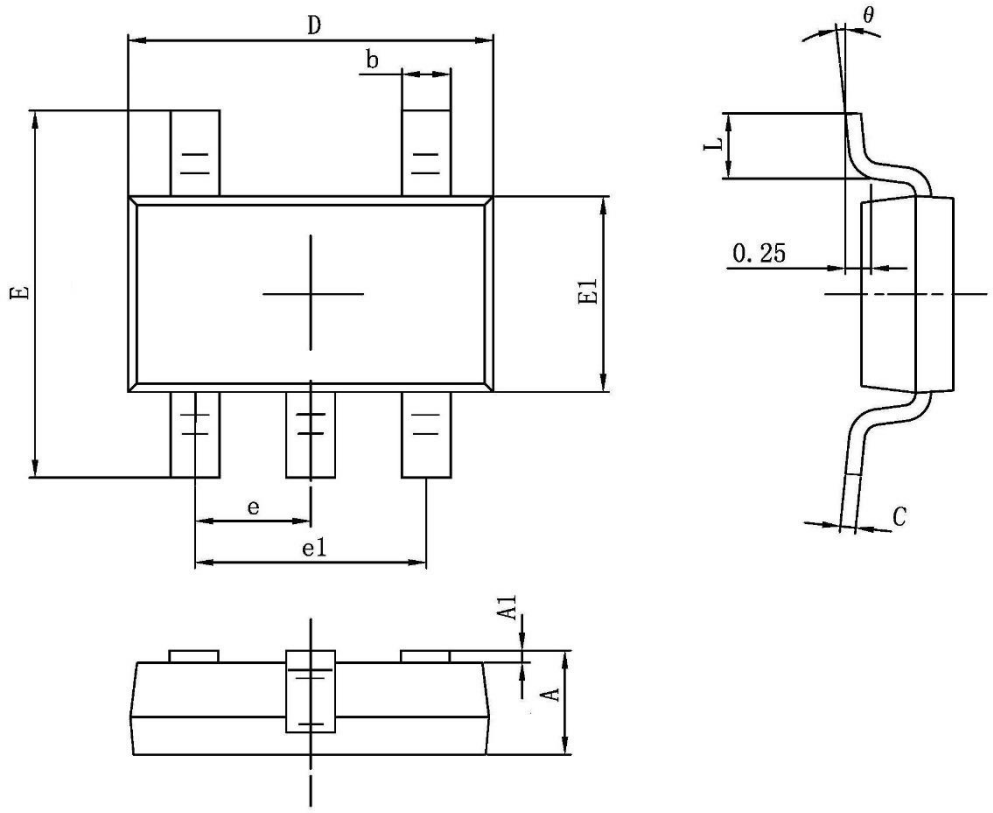


Symbol	MIN	NOM	MAX
A	1.350	1.550	1.750
A1	0.050	0.150	0.250
b	0.330	0.420	0.510
c	0.150	0.200	0.250
D	4.700	4.925	5.150
E1	3.700	3.900	4.100
E	5.800	6.000	6.200
e		1.270(BSC)	
L	0.400	0.650	0.900
θ	0°	4°	8°

NOTE:

1. **Dimensions are in Millimeters.**

SOT23-5L



Symbol	MIN	NOM	MAX
A	1.030	1.140	1.250
A1	0.003	0.050	0.110
b	0.330	0.370	0.410
c	0.130	0.150	0.170
D	2.800	2.900	3.000
E1	1.500	1.600	1.700
E	2.600	2.800	3.00
e	0.950(BSC)		
e1	1.900(BSC)		
L	0.300	0.450	0.600
θ	0°	4°	8°

NOTE:

1. **Dimensions are in Millimeters.**

Revision History

Version	Publication date	Pages	Revise Description
1.0	Mar. 2025	21	Initial document Release.

Sales and Service

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